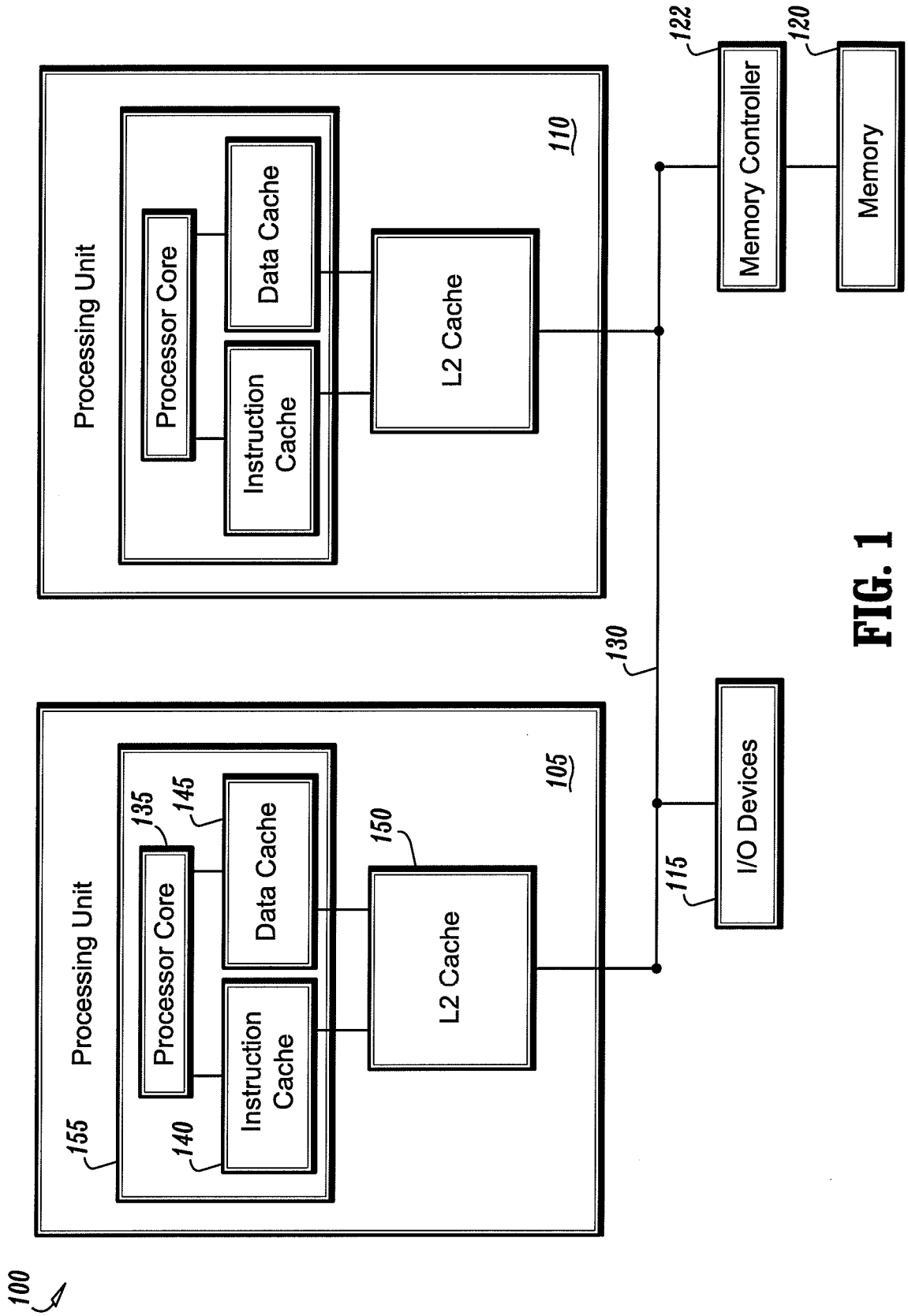

FIG. 1
(Prior Art)

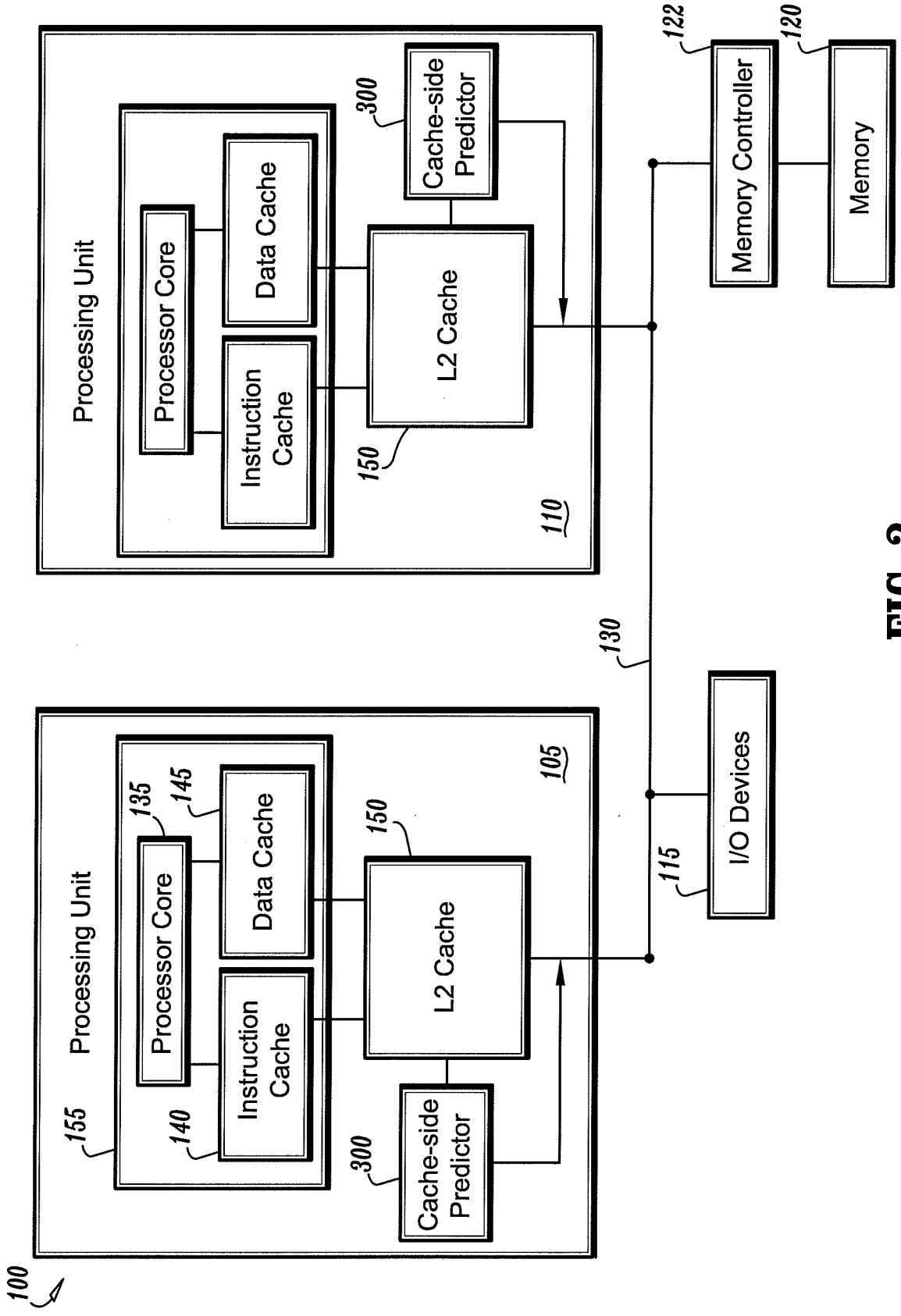
100
Processing Unit
155
Processor Core
140
Instruction Cache
135
145
Data Cache
150
L2 Cache
300
Cache-side Predictor
105
Processing Unit
Processor Core
Instruction Cache
Data Cache
300
Cache-side Predictor
150
L2 Cache
110
130
115
I/O Devices
122
Memory Controller
120
Memory

FIG. 2

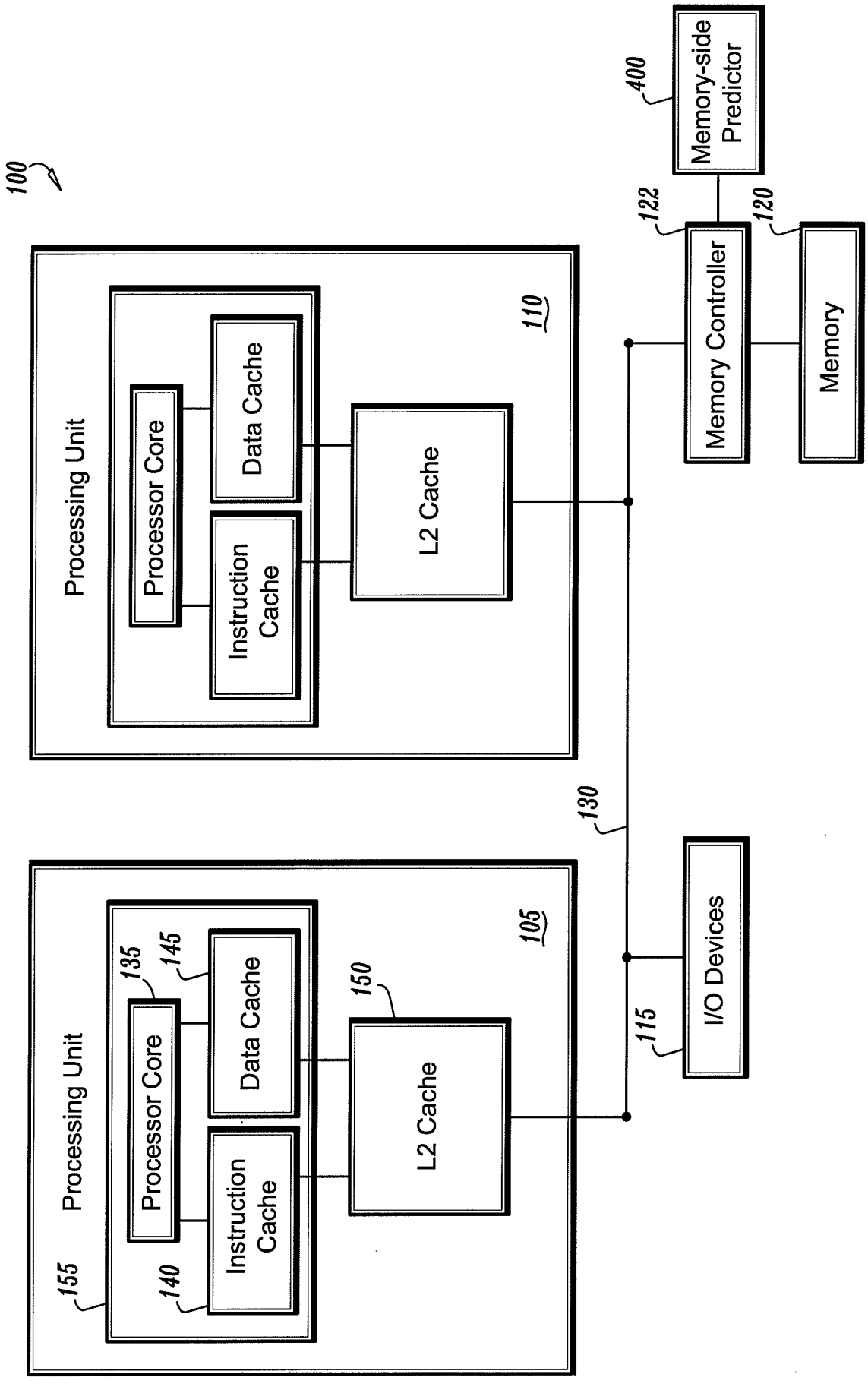
100
Processing Unit
Processor Core
Data Cache
Instruction Cache
L2 Cache
110
Processing Unit
Processor Core
Data Cache
Instruction Cache
L2 Cache
105
135
145
150
140
155
130
115
I/O Devices
Memory Controller
Memory
122
120
Memory-side Predictor
400

FIG. 3

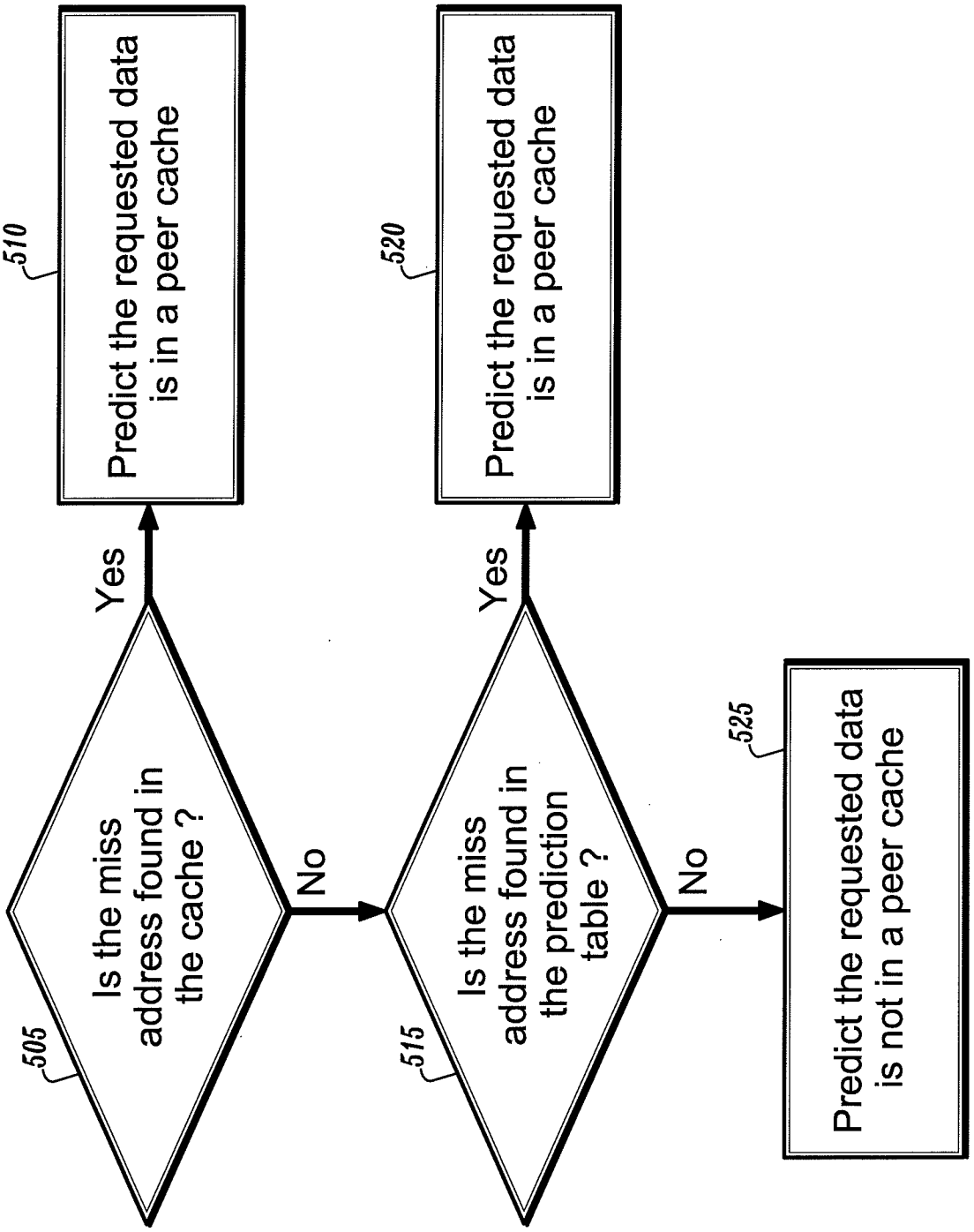
505
Is the miss address found in the cache ?
Yes
510
Predict the requested data is in a peer cache
No
515
Is the miss address found in the prediction table ?
Yes
520
Predict the requested data is in a peer cache
No
525
Predict the requested data is not in a peer cache

FIG. 4

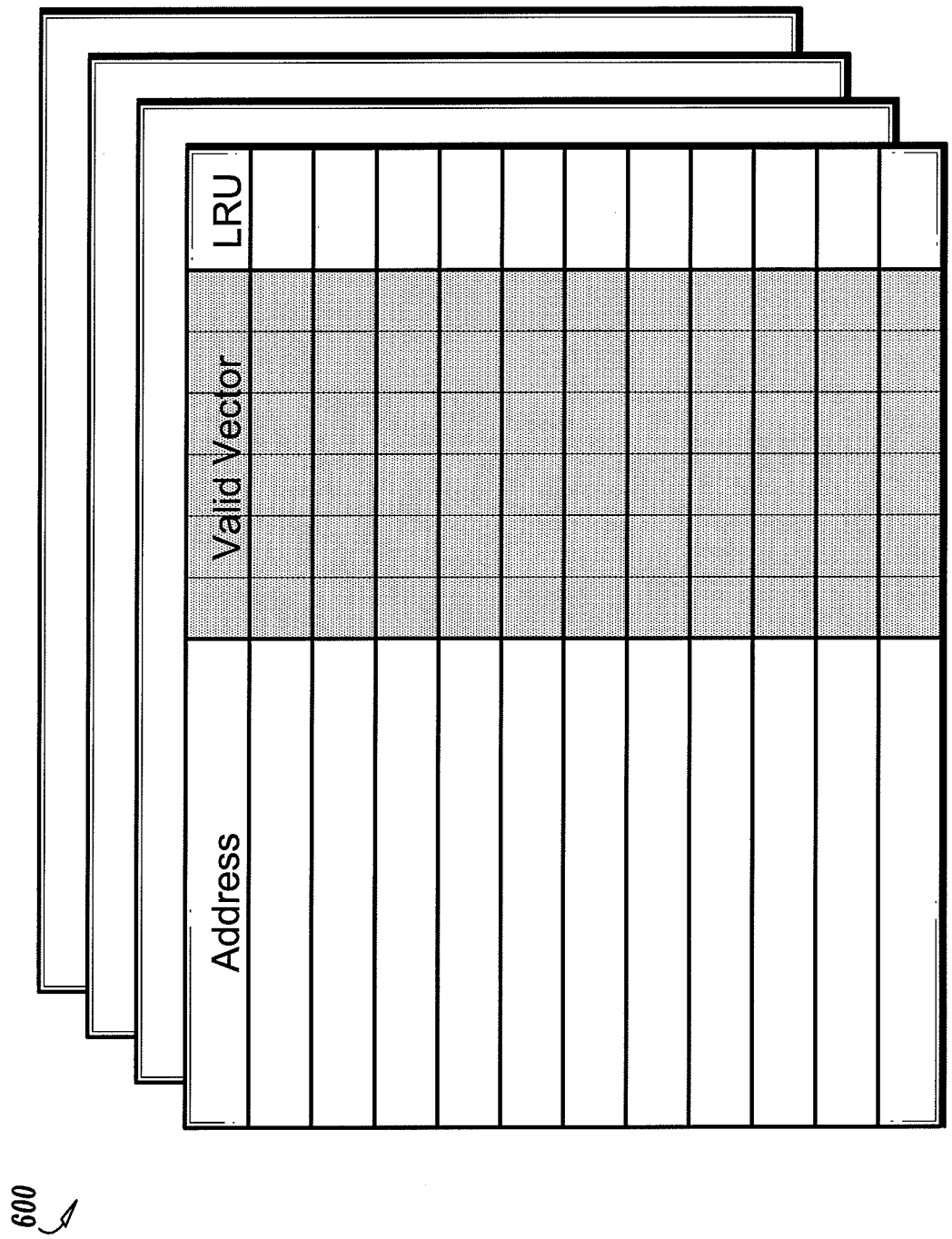

FIG. 5

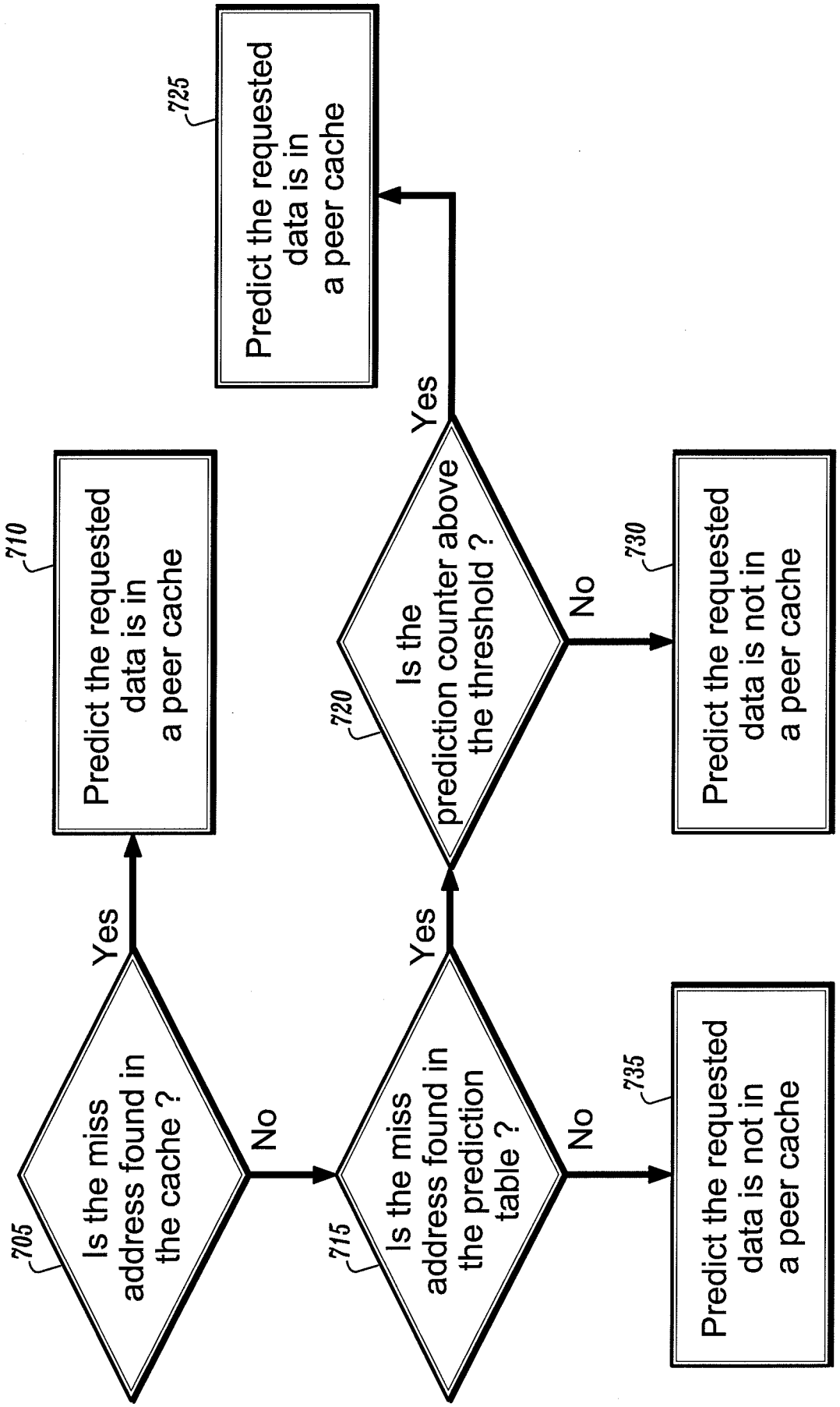
705
Is the miss address found in the cache ?
Yes
710
Predict the requested data is in a peer cache
No
715
Is the miss address found in the prediction table ?
Yes
720
Is the prediction counter above the threshold ?
Yes
725
Predict the requested data is in a peer cache
No
730
Predict the requested data is not in a peer cache
No
735
Predict the requested data is not in a peer cache

FIG. 6

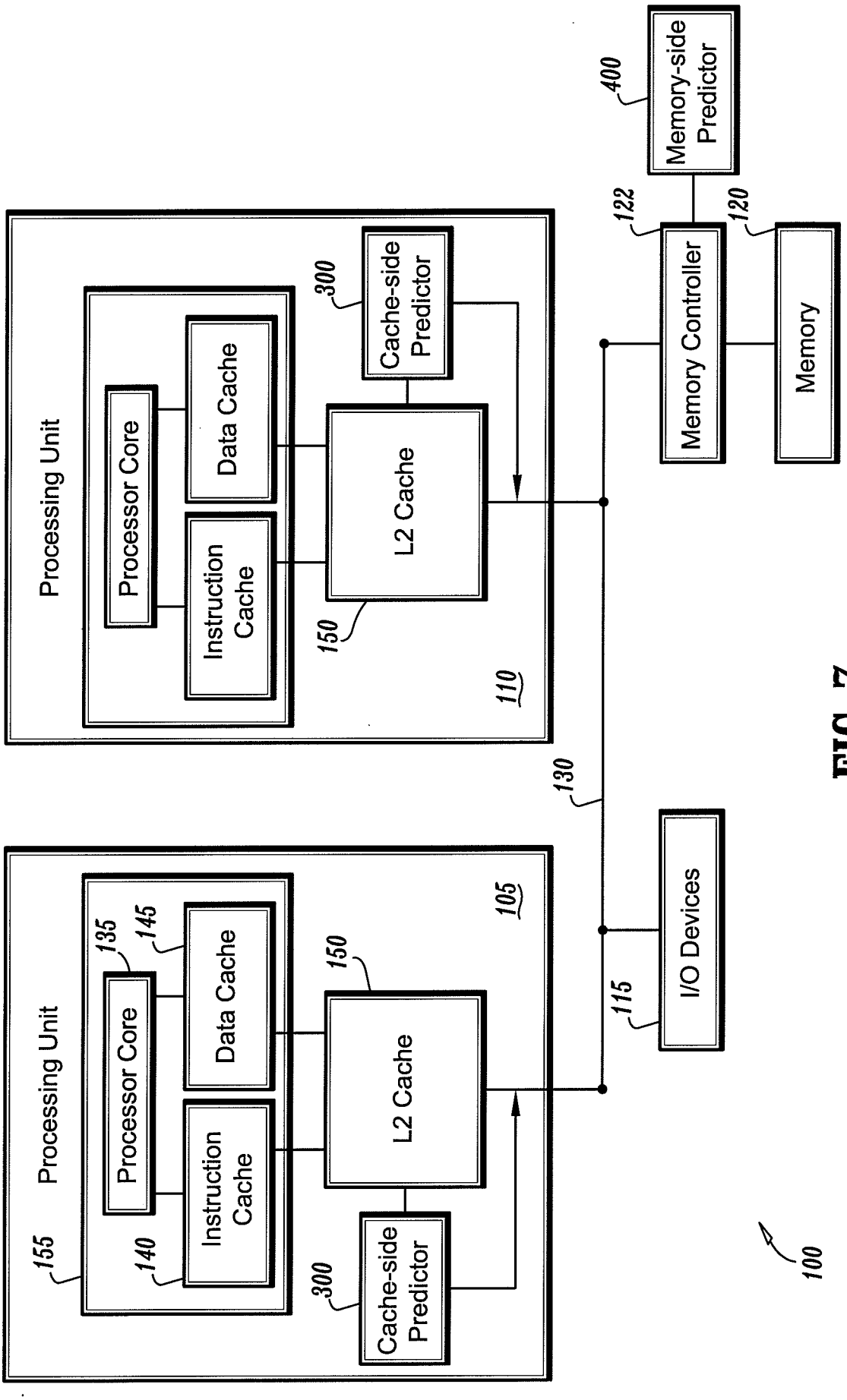
Memory-side Predictor
400
122
120
Memory Controller
Memory
Processing Unit
Processor Core
Data Cache
Instruction Cache
Cache-side Predictor
300
L2 Cache
150
110
130
I/O Devices
115
105
135
145
140
155
100

FIG. 7